WHAT IS CLAIMED IS:

1. A semiconductor interconnect structure, comprising:

a conductive structure on a substrate;

a first dielectric layer over the conductive structure; and

an etching stop layer over the first dielectric layer, wherein at least a portion of sidewalls of the conductive structure are surrounded by first level air gaps, an opening disposed over part of a surface of the conductive structure, wherein the first level air gaps are isolated from the opening.

2. The interconnect structure of claim 1, wherein the conductive structure comprises a aluminum, copper, tungsten, polysilicon, metal, and metal alloy thereof.

3. The interconnect structure of claim 1, wherein the material of the first dielectric layer and the etching stop layer are different.

4. The interconnect structure of claim 1, wherein the etching selectivity of the first dielectric layer with respect to the etching stop layer is substantially high.

5. The interconnect structure of claim 1, wherein the first dielectric layer comprises silicon oxide.

6. The interconnect structure of claim 1, wherein the first dielectric layer comprises doped oxide.

7. The interconnect structure of claim 1, wherein the first dielectric layer is formed by using a plasma enhanced chemical vapor deposition method (PECVD).

8. The interconnect structure of claim 1, wherein the etching stop layer comprises silicon nitride.

9. The interconnect structure of claim 1, wherein the etching stop layer comprises silicon nitride, aluminum oxide, aluminum nitride, titanium oxide, silicon carbide, and aluminum silicate.

10. The interconnect structure of claim 1, wherein the etching stop layer is formed by using a plasma enhanced chemical vapor deposition method (PECVD).

11. The interconnect structure of claim 1, wherein the etching stop layer is formed by using a photo-induced chemical vapor deposition (PICVD).

12. The interconnect structure of claim 1, wherein the level of the top surface of the conductive structure is higher than a level of an interface between the first level air gaps and the first dielectric layer corresponding to a level between the conductive structure and the substrate.

13. The interconnect structure of claim 1, wherein a height of an interface between the first level air gaps and the substrate is lower than a height of an interface between the conductive structure and the substrate.

14. The interconnect structure of claim 1, wherein the width of the opening is substantially equal to the width of the conductive structure.

15. The interconnect structure of claim 1, further comprising a second dielectric layer disposed over the first dielectric layer and the etching stop layer, wherein the opening exposes the conductive structure through the first dielectric layer and the second dielectric layer.

16. The interconnect structure of claim 15, wherein the second dielectric layer comprises silicon oxide.

17. A semiconductor interconnect structure, comprising:

a conductive structure having a top surface and a side surface;

a first dielectric layer over the conductive structure, wherein the side surface of the conductive structure is surrounded by first level air gaps and an upper portion of the side surface is surrounded by the first dielectric layer;

an etching stop layer over the first dielectric layer, wherein the etching stop layer is disposed over the first level air gaps; and

an opening disposed over the top surface and part of the upper portion of the side surface of the conductive structure, wherein the first level air gaps are isolated from the opening by the etching stop layer.

18. The interconnect structure of claim 17, wherein the conductive structure comprises a aluminum, copper, tungsten, polysilicon, metal, and metal alloy thereof.

19. The interconnect structure of claim 17, wherein the material of the first dielectric layer and the etching stop layer are different.

20. The interconnect structure of claim 17, wherein the etching selectivity of the first dielectric layer with respect to the etching stop layer is substantially high.

21. The interconnect structure of claim 17, wherein the first dielectric layer comprises silicon oxide.

22. The interconnect structure of claim 17, wherein the first dielectric layer comprises doped oxide.

23. The interconnect structure of claim 17, wherein the first dielectric layer is formed by using a plasma enhanced chemical vapor deposition method (PECVD).

24. The interconnect structure of claim 17, wherein the etching stop layer comprises silicon nitrides.

25. The interconnect structure of claim 17, wherein the etching stop layer comprises silicon nitride, aluminum oxide, aluminum nitride, titanium oxide, silicon carbide, and aluminum silicate.

26. The interconnect structure of claim 17, wherein the etching stop layer is formed by using a plasma enhanced chemical vapor deposition method (PECVD).

27. The interconnect structure of claim 17, wherein the etching stop layer is formed by using a photo-induced chemical vapor deposition (PICVD).

28. The interconnect structure of claim 17, further comprising a second dielectric layer disposed over the first dielectric layer and the etching stop layer, wherein the opening exposes the conductive structure through the first dielectric layer and the second dielectric layer.

29. The interconnect structure of claim 28, wherein the second dielectric layer comprises silicon oxide.

30. The interconnect structure of claim 17, wherein the level of the top surface of the conductive structure is higher than a level of an interface between the first level air gaps and the first dielectric layer corresponding to a level between the conductive structure and the substrate.

31. The interconnect structure of claim 17, wherein a height of an interface between the first level air gaps and the substrate is lower than a height of an interface between the conductive structure and the substrate.

32. The interconnect structure of claim 17, wherein the width of the opening is substantially equal to the width of the conductive structure.

33. A semiconductor interconnect structure, comprising:

a conductive structure on a substrate;

a cap layer disposed on the conductive structure; and

a first dielectric layer over the conductive structure, wherein at least a portion of sidewalls of the conductive structure and the cap layer are surrounded by first level air gaps, an opening disposed over at least part of a surface of the conductive structure, wherein the first level air gaps are isolated from the opening.

34. The interconnect structure of claim 33, wherein the conductive structure comprises a aluminum, copper, tungsten, polysilicon, metal, and metal alloy thereof.

35. The interconnect structure of claim 33, wherein the material of the cap layer comprises doped dielectric.

36. The interconnect structure of claim 33, wherein the material of the cap layer and the first dielectric layer are different.

37. The interconnect structure of claim 33, wherein the etching selectivity of the cap layer with respect to the first dielectric layer is substantially high.

38. The interconnect structure of claim 33, wherein the first dielectric layer comprises silicon oxide.

39. The interconnect structure of claim 33, wherein the first dielectric layer comprises doped oxide.

40. The interconnect structure of claim 33, wherein the first dielectric layer is formed by using a plasma enhanced chemical vapor deposition method (PECVD).

41. The interconnect structure of claim 33, further comprising a second dielectric layer disposed over the first dielectric layer, wherein the opening exposes the conductive structure through the first dielectric layer and the second dielectric layer.

42. The interconnect structure of claim 41, wherein the second dielectric layer comprises silicon oxide.

43. The interconnect structure of claim 33, wherein the level of the top surface of the conductive structure is lower than a level of an interface between the first level air gaps and the first dielectric layer corresponding to a level between the conductive structure and the substrate.

44. The interconnect structure of claim 33, wherein a height of an interface between the first level air gaps and the substrate is higher than a height of an interface between the conductive structure and the substrate.

45. The interconnect structure of claim 33, wherein the width of the opening is substantially equal to the width of the conductive structure.

46. The interconnect structure of claim 33, further comprising a layer over the first dielectric layer, wherein the layer is disposed over the first level air gaps and the opening disposed over at least a portion of the layer.

47. The interconnect structure of claim 46, the width of the layer is substantially equal to the width of the opening.

48. A semiconductor interconnect structure, comprising:

a conductive structure on a substrate;

a cap layer disposed on a portion of a top surface of the first conductive level conductive structure, the cap layer having a top surface, a first side surface and a second side surface, wherein the conductive structure and a lower portion of the first side surface of the cap layer are surrounded by first level air gaps and an upper portion of the first side is surrounded by the a first dielectric layer; and

an opening disposed over an upper portion of the conductive structure, the second side surface of the cap layer, and a portion of the first dielectric layer, wherein the first level air gaps are isolated from the opening by the first dielectric layer.

49. The interconnect structure of claim 48, wherein the conductive structure comprises a aluminum, copper, tungsten, polysilicon, metal, and metal alloy thereof.

50. The interconnect structure of claim 48, wherein the material of the cap layer comprises doped dielectric.

51. The interconnect structure of claim 48, wherein the material of the cap layer and the first dielectric layer are different.

52. The interconnect structure of claim 48, wherein the etching selectivity of the cap layer with respect to the first dielectric layer is substantially high.

53. The interconnect structure of claim 48, wherein the first dielectric layer comprises silicon oxides.

54. The interconnect structure of claim 48, wherein the first dielectric layer comprises doped oxides.

55. The interconnect structure of claim 48, wherein the first dielectric layer is formed by using a plasma enhanced chemical vapor deposition method (PECVD).

56. The interconnect structure of claim 48, further comprising a second dielectric layer disposed over the first dielectric layer, wherein the opening exposes the conductive structure through the first dielectric layer and the second dielectric layer.

57. The interconnect structure of claim 56, wherein the second dielectric layer comprises silicon oxides.

58. The interconnect structure of claim 48, wherein the level of the top surface of the conductive structure is lower than a level of an interface between the first level air gaps and the first dielectric layer corresponding to a level between the conductive structure and the substrate.

59. The interconnect structure of claim 48, wherein a height of an interface between the first level air gaps and the substrate is higher than a height of an interface between the conductive structure and the substrate.

60. The interconnect structure of claim 48, wherein the width of the opening is substantially equal to the width of the conductive structure.

61. The interconnect structure of claim 48, further comprising a layer over the first dielectric layer, wherein the layer is disposed over the first level air gaps and the opening disposed over a portion of the layer.

62. The interconnect structure of claim 48, the width of the layer is substantially equal to the width of the opening.

63. A semiconductor interconnect structure, comprising:

a pair of conductive structures;

a first dielectric layer over the conductive structures, wherein a first level air gap disposed between the conductive structures in the first dielectric layer; and

an opening disposed over at least part of the conductive structure, wherein the first level air gap is isolated from the opening.

64. The interconnect structure of claim 63, further comprising an etching stop layer over the first dielectric layer, and substantially disposed over the first level air gap, wherein the first level air gap is isolated from the opening by the etching stop layer.

65. The interconnect structure of claim 64, wherein the etching selectivity of the first dielectric layer with respect to the etching stop layer is substantially high.

66. The interconnect structure of claim 63, further comprising a cap layer disposed on a portion of a top surface of the first conductive level conductive structure, the cap layer having a top surface, a first side surface and a second side surface, the first

side surface having a lower portion beside the first level air gap and an upper portion surrounded by a first dielectric layer; the opening disposed over the second side surface of the cap layer and isolated from the first level air gap.

67. The interconnect structure of claim 66, further comprising an etching stop layer over the first dielectric layer, and substantially disposed over the first level air gap, wherein the first level air gap is isolated from the opening by the etching stop layer.

68. The interconnect structure of claim 67, wherein the etching selectivity of the first dielectric layer with respect to the etching stop layer is substantially high.

69. A semiconductor interconnect structure, comprising:

a pair of conductive structures, wherein an air gap disposed between the conductive structures; and

a dielectric layer over the conductive structures, the dielectric layer having a stop layer disposed over the air gap, wherein the dielectric layer has an opening exposing a portion of the conductive structure and being isolated from the air gap.

70. The interconnect structure of claim 69, wherein the etching selectivity of the dielectric layer with respect to the stop layer is substantially high.

71. The interconnect structure of claim 69, further comprising a cap layer disposed on a portion of a top surface of the conductive structure, the cap layer having a top surface, a first side surface and a second side surface, the first side surface having a lower portion beside the air gap and an upper portion surrounded by the dielectric layer, the opening being disposed over the second side surface of the cap layer and isolated from the air gap.

72. A semiconductor interconnect structure, comprising:

a pair of conductive structures, wherein an air gap disposed between the conductive structures; and

a dielectric layer over the conductive structures, the dielectric layer having a stop layer disposed over the air gap, wherein the dielectric layer has an opening disposed over at least a portion of the conductive structure and at least a top portion of the stop layer, the opening being isolated from the air gap.

73. The interconnect structure of claim 72, wherein the etching selectivity of the dielectric layer with respect to the stop layer is substantially high.

74. The interconnect structure of claim 72, further comprising a cap layer disposed on a portion of a top surface of the conductive structure, the cap layer having a top surface, a first side surface and a second side surface, the first side surface having a lower portion beside the air gap and an upper portion surrounded by the dielectric layer, the opening being disposed over the second side surface of the cap layer and isolated from the air gap.

75. A semiconductor interconnect structure, comprising:

a substrate;

a pair of conductive structures, wherein an air gap disposed between the conductive structures; and

a dielectric layer over the substrate, having an air gap formed within, the air gap disposed between the conductive structures;

a stop layer disposed over the air gap; and

an opening disposed over at least part of the stop layer and at least part of the conductive layer, wherein the air gap is isolated from the opening.